公司介绍

LTRIN

2018. 07. 09

1. 事业项目及市场

2. LTRIN及保有技术介绍

3. 在中国业务战略

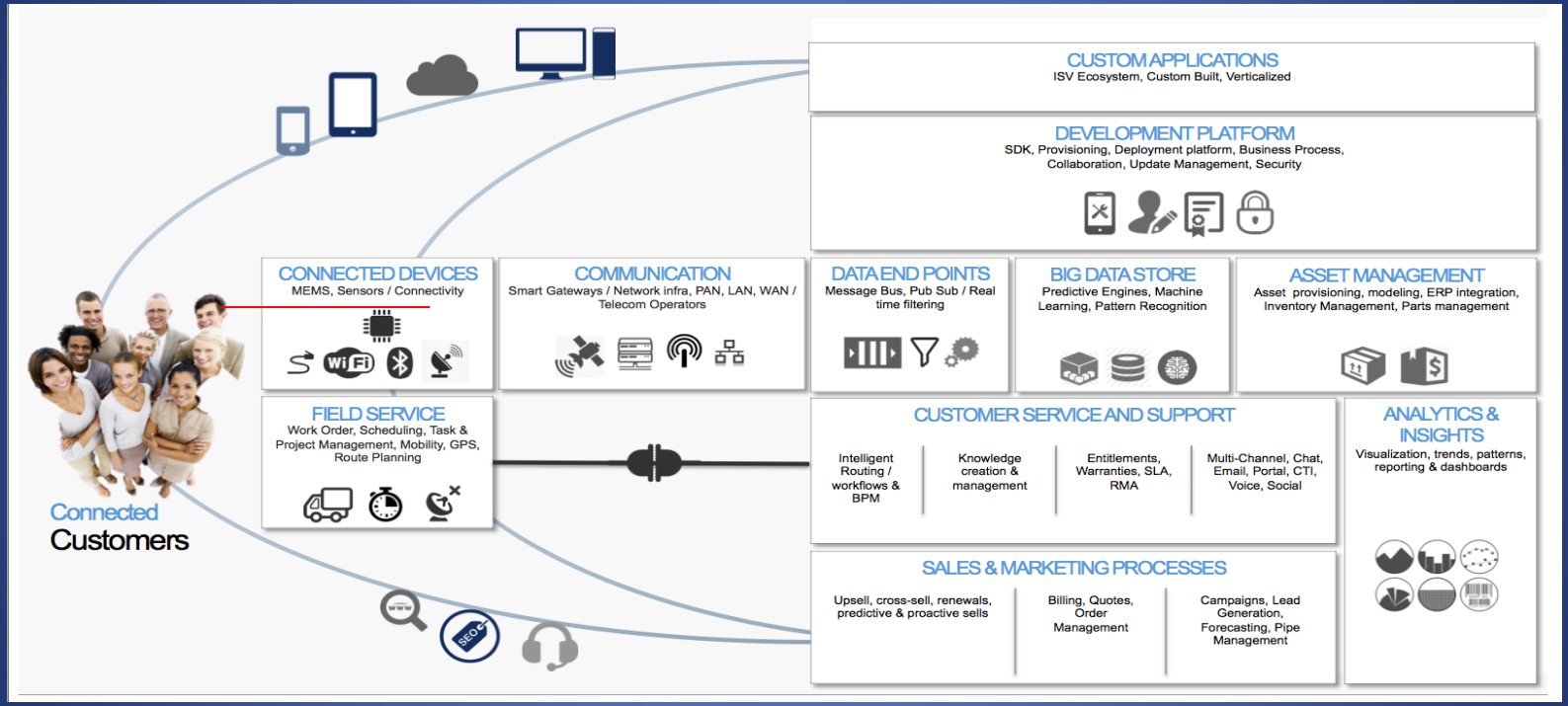
事业项目及市场

第4次产业核心领域

物联网　　无人汽车

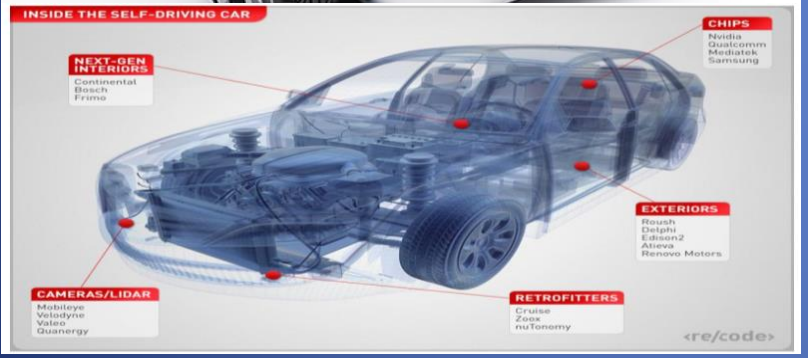
人工智能　　微型LED

物联网和传感器



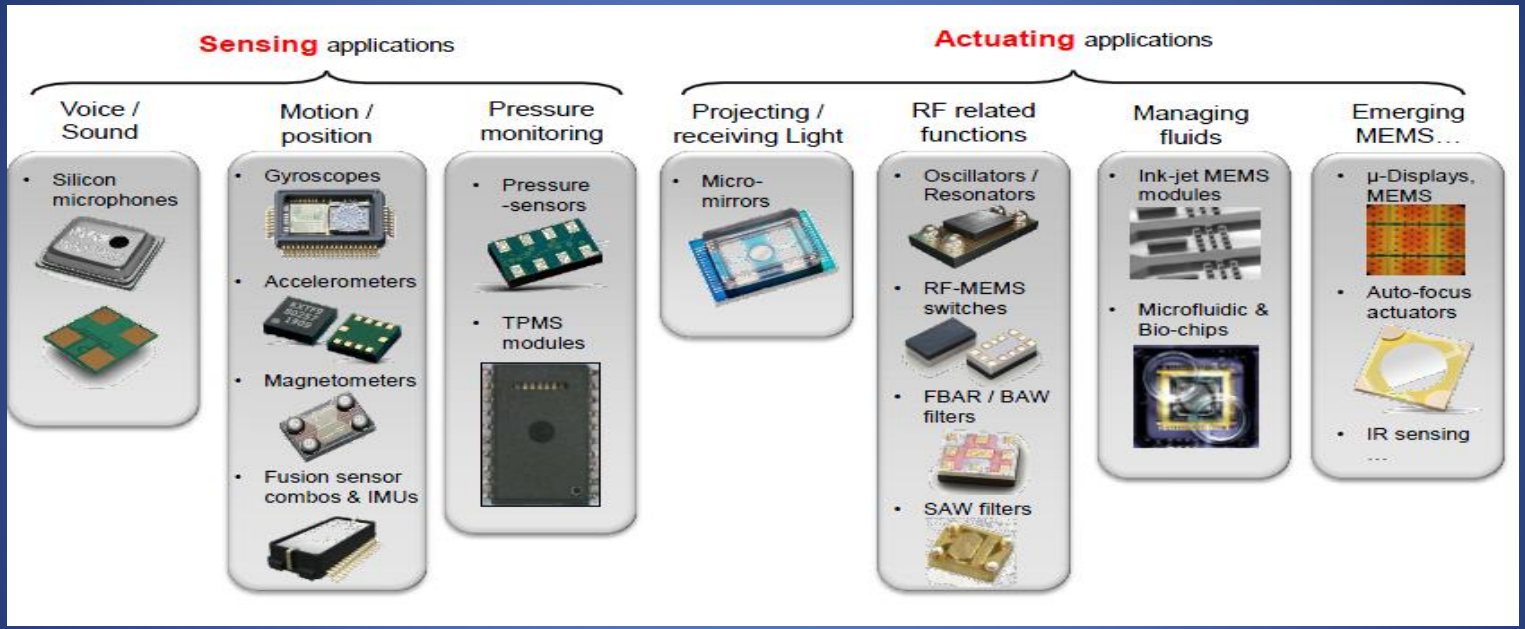
物联网 为了做，需要很多传感器

无人自动化和传感器



无人自动化时代即将到来, 为此需要很多传感器.

MEMS技术和传感器

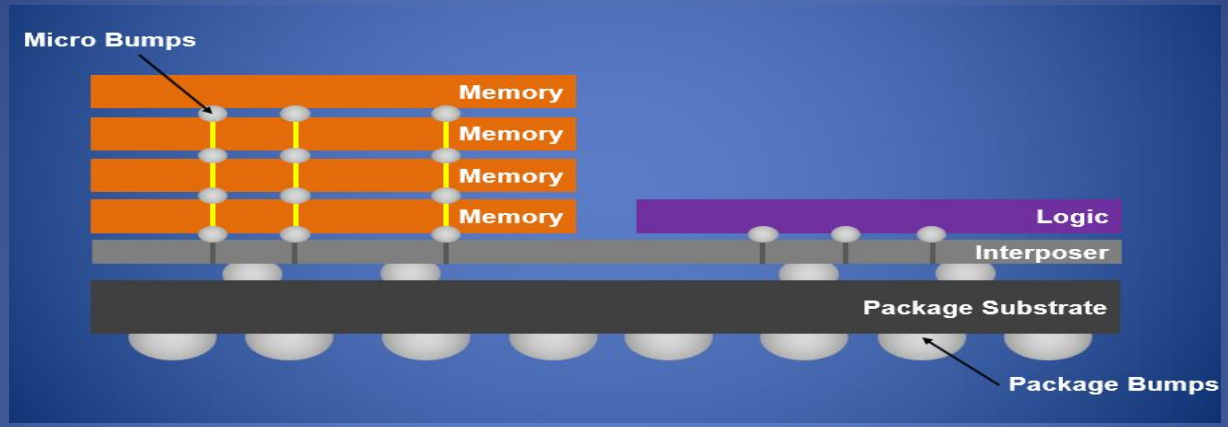


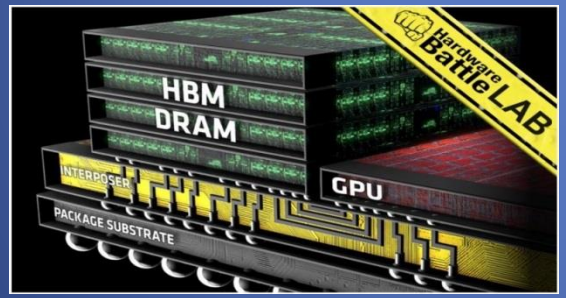
MEMS : Micro-Electro-Mechanical Systems

来源：Yole Development

所有传感器均采用MEMS技术 因此预计MEMS制作用设备的需求量将会最大

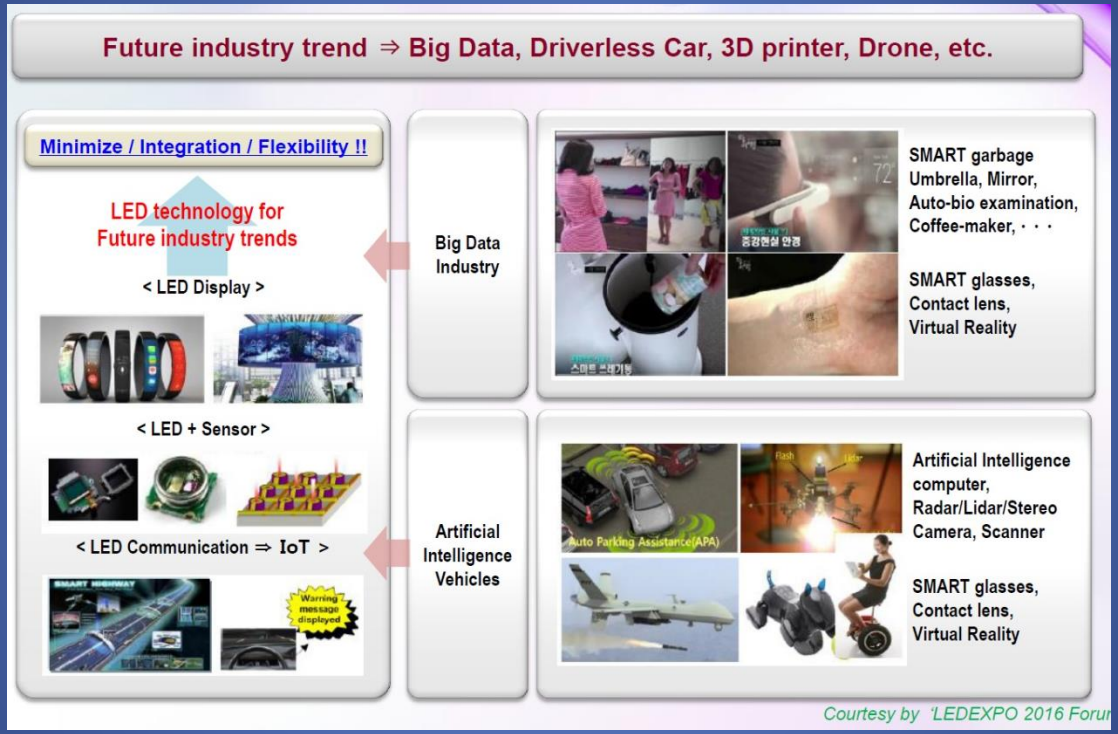
2.5D and HBM





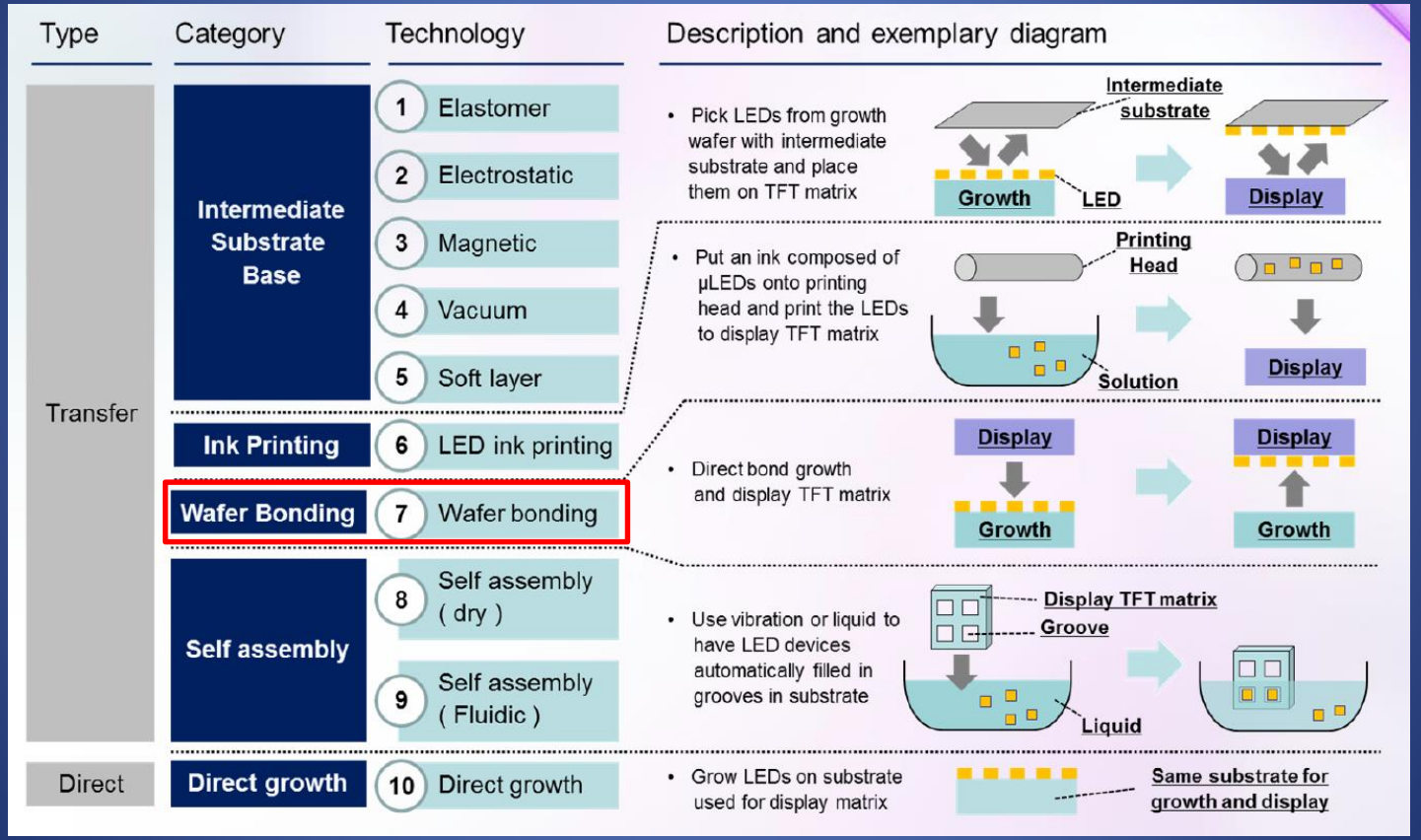
为了制作高性能储存器材2.5半导体制造技术正全面批量生产

微型LED业务领域

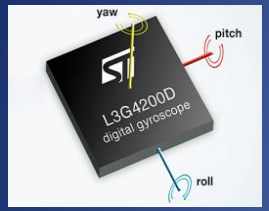


对全球新一代的显示器正在迅速崛起为微型LED的投资大幅增加

微型LED核心制造技术

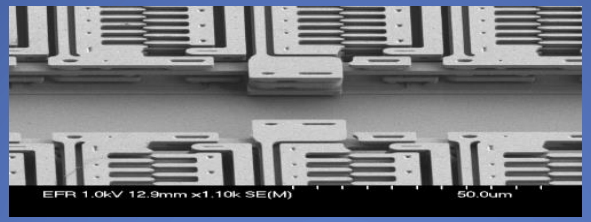


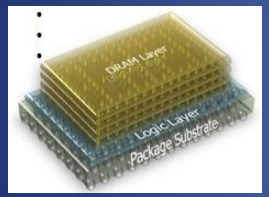
核心制造工序



MEMS

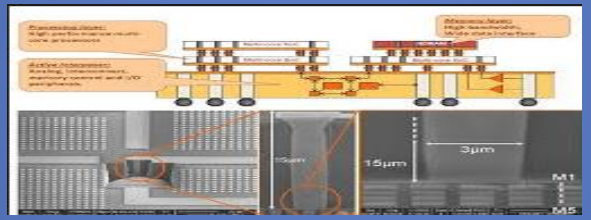
传感器



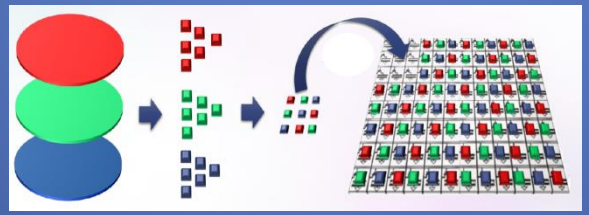


2.5D

半导体



显示屏



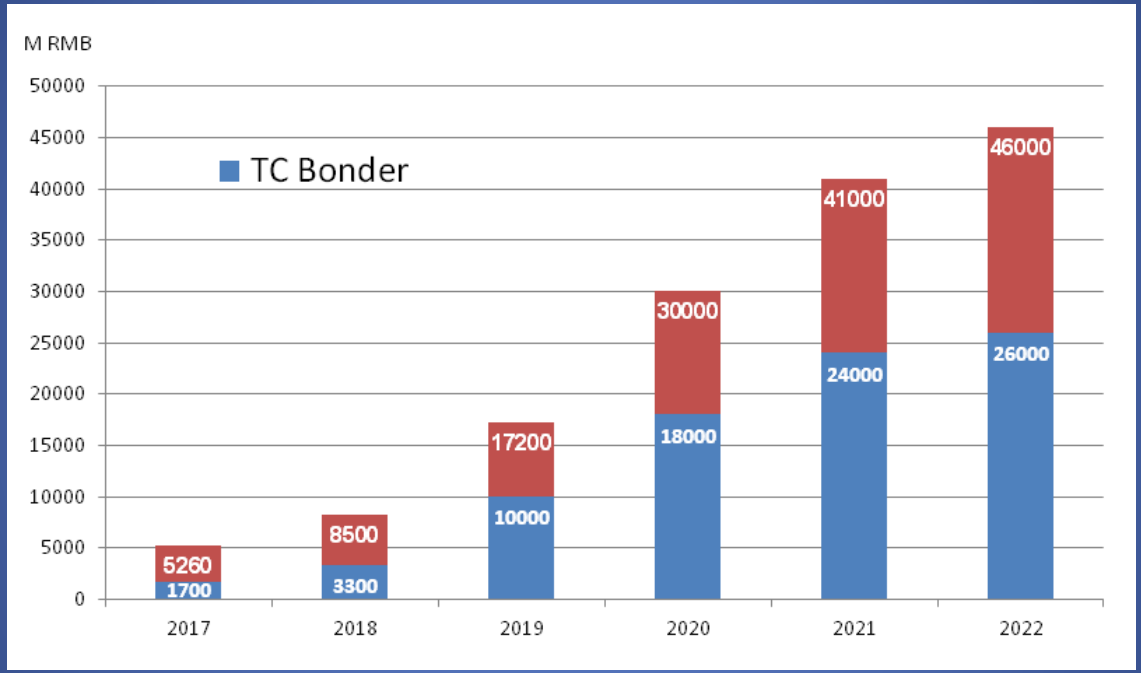
核心技术

晶圆键合

晶圆键合是为物联网、无人驾驶所需的各式传感器，

2.5半导体器材、新一代显示器制造所需的核心技术！

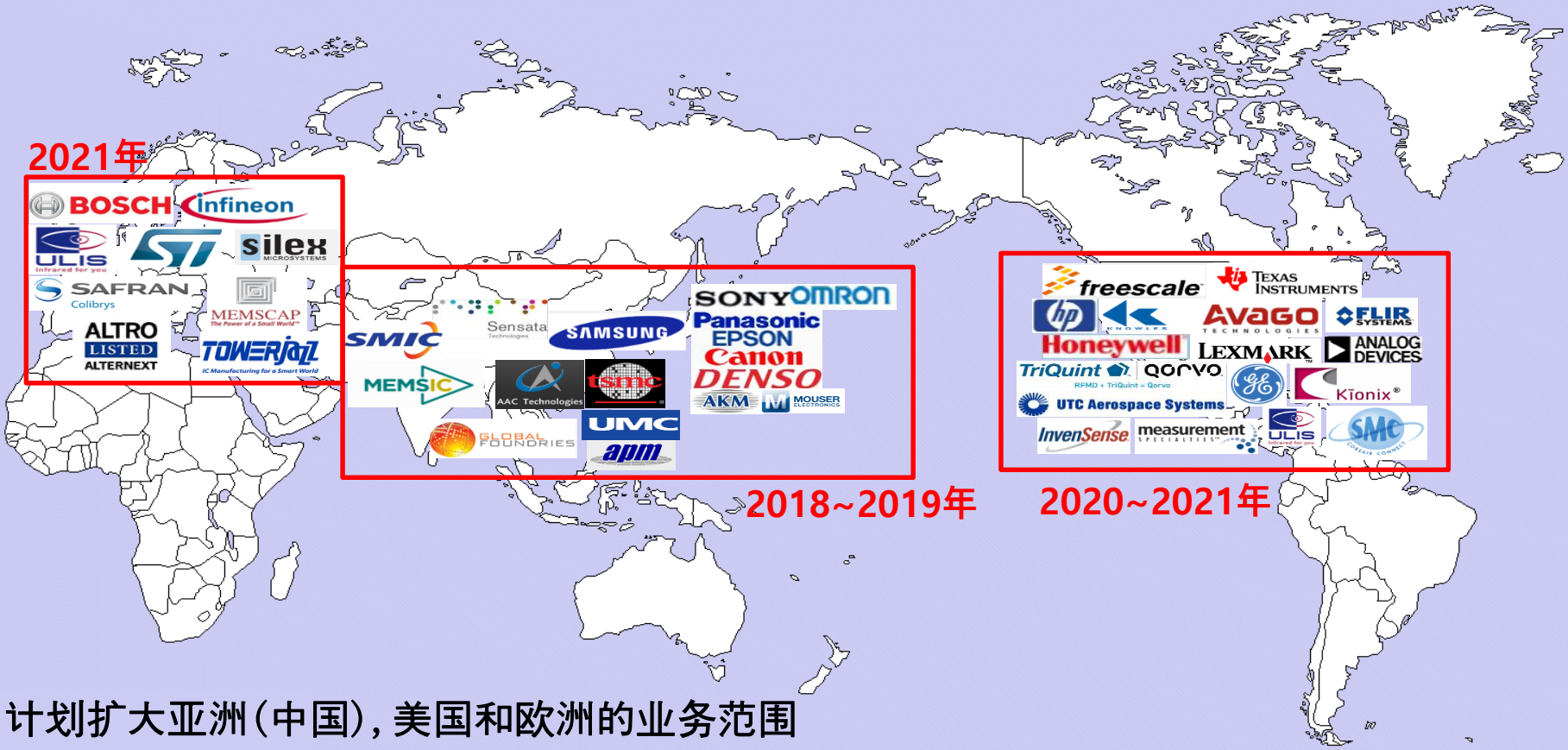
Wafer Bonder 市场



2020年, 预计晶圆键合机整体市场规模约达31,000,000,000 RMB,

TC热压键合机市场规模约达 18,000,000,000 RMB.

客户



计划扩大亚洲(中国),美国和欧洲的业务范围

LTRIN及保有技术介绍

公司概述

建立	2007年6月
业务	MEMS、CIS和3D集成的晶圆连接器。 (Wafer Bonder for MEMS, CIS and 3D Integration)
技术	射频加热 (RF Heating) 现场调整和焊接 (In-situ Align and Bonding) 晶片表面处理 (Wafer Surface Treatment)
专利	国际3项/国内14项 (International 3 / Domestic 14)
联系	Tel +82-31-627-2572~3

办公室

制造 Clean Room

试验 Clean Room

公司沿革

2017	Start the Product evaluation for micro LED Project with LG Display AR/VR Team
2016	Supply 6 inch RF Heater for Wearable Device – Wonik IPS
2015	Development of 8 inch Thermocompressive Wafer Bonder for MEMS and WLP
2014	Supply 6 inch Thermocompressive Wafer Bonder for UV-LED and Lighting – LG innotek
2012	Awarded the Government project (300mm BSI-CIS Wafer Bonder) INNO-BIZ. Company Awarded
2011	Awarded the Government Project (Thermocompressive Bonder for LED) Supply 6 inch RF Thermocompressive Bonder for LED
2010	Supply 8 inch Thermocompressive Wafer Bonder for 3D-CIS to Samsung System LSI Awarded the Government Project (High Brightness vertical LED Wafer Bonder)
2008	Supply 12 inch Wafer Direct Bonder for SOI - Charm Engineering R&D Lab. Establishment
2007	LTrin Establishment

专利

号码	注册编号	专利编号	题目
1	2007-0097037	10-0936778	Wafer Bonding Method
2	2007-0097038	10-0893182	Wafer Cleaning Method
3	2008-0021513	10-0980045	Substrates Bonding Method
4	2008-0038202	10-0872908	Apparatus for Substrate Surface Treatment
5	2008-0038204	10-0886957	Substrate Bonding Module and Method using the same
6	12/602,285 (US)	US 8,278,186 B2	Wafer Cleaning Method and Wafer Bonding Method using the same
7	2010-0011642	10-1017361	Substrate Bonding System and Mobile Chamber used Thereto
8	2010-0067798	10-1165784	Epitaxial Wafer Package and Fabrication Method using the same
9	10-2011-0070115	10-1544895	Apparatus for Adjusting Coil and Substrate Bonding Chamber using the same
10	2011-0109796	10-1268898	Apparatus for bonding substrates and method of bonding substrates
11	13/577,458 (US)	US 8,999,099 B2	Substrate Bonding System and Mobile Chamber used Thereto
12	61/817,624 (US)		Apparatus and method for bonding substrates
13	10-2013-0130622	10-1621792	Apparatus for substrates bonding
14	10-2014-0059256	10-1608921	Apparatus for substrates bonding
15	10-2014-0064394	10-1621777	Apparatus and method for substrates bonding
16	10-2014-0064395	10-1580206	Apparatus for substrates bonding
17	10-2016-0102538		Wafer bonder and coil block apparatus using electromagnetic wave heating

Overseas patent pending : 1
Overseas patent : 2
Domestic patent pending : 1
Domestic patent : 13

Total 17

董事长介绍

CEO Name **Yong-Won, Cha** 24 years experience in the semiconductor field

Aug/09 ~ Present LTrin CO., LTD. ***CEO***

- 6" RF Heater for Wearable Device (Wonik IPS)
- 6" Thermocompressive Wafer Bonder for LED (LG Innotek)
- 8" Thermocompressive Wafer Bonder for MEMS and V-LED (Chung-Ang Univ.)
- 8" Thermocompressive Wafer Bonder for 3D-CIS (Samsung Electronics)

Feb/08 ~ July/09 ITI Ventures ***President***

- Technical consultant for VSEA (Applied Materials,USA)

July/02 ~ Jan/08 SAMSUNG ELEC. CO., LTD. ***Senior Engineer –Process Development Team, Memory R&D Division***

- Controlled the full process schemes to make Si active layers using the layer transfer technologies in stacked devices and set the base processes such as H implantation, wafer bonding and cleaving key development items for stacked devices, especially stacked Flash memory for 64G or 128G density. (2 patent)
- Developed and implemented a new STI method utilizing new structural concepts and processes to enhance the reliabilities including retention, endurance and HTS properties and to cut costs through simple STI structure in the Flash memory. (2 patents)
- Created and evaluated a new HDP-CVD process for Silicon-rich Oxide as a discrete charge storage medium of non-volatile memory cell that is one of the key technologies in sub-50nm device and beyond. (Published at IEDM and MRS, 1 patent)
- Developed various HDP-CVD processes such as NF_3-HDP, H_2-HDP and H_2-PSG for DRAM, SRAM and Flash Memory using Design of Experiments and set those procedures standard conditions for sub-90nm technology devices. (Published at VLSI, 3 patents)
- Conceived various gap-filling processes for STI, ILD and IMD layers and successfully transferred the key gap-filling methods to the mass production line using 300mm wafers.

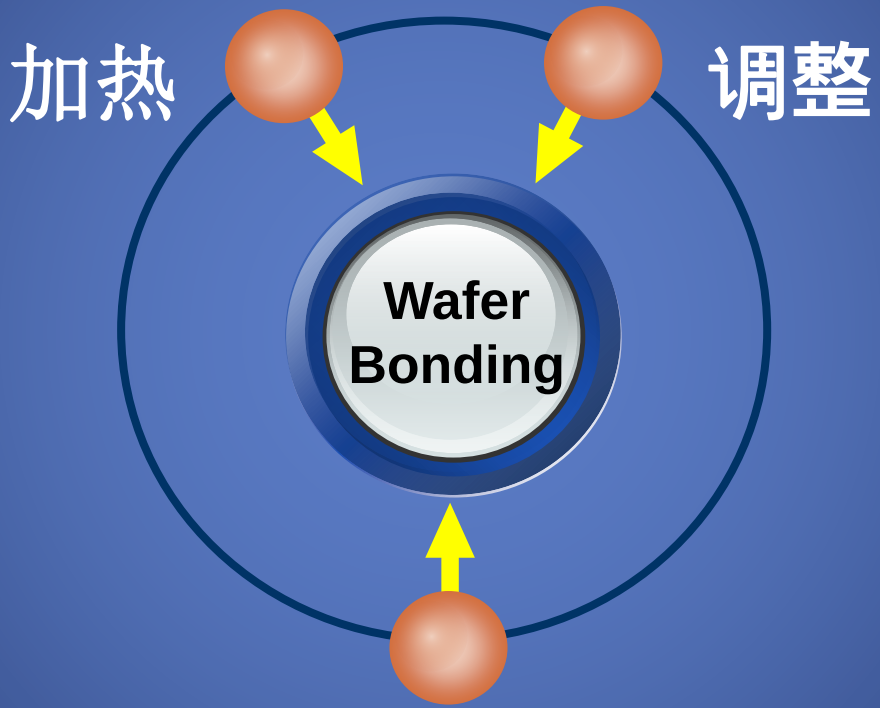
June/97 ~ June/01 Hynix Semiconductor Inc. ***Assistant Manager – Advanced Process Team, Memory R&D Division***

- Spearheaded the dielectric thin film part in the Task Force Team for 512 Mb DDR DRAM development using 0.13㎛ technology and transferred key CVD processes to the mass production line successfully.
- Successfully launched HDP-CVD processes at STI, ILD and IMD layers in the Task Force Team for the purpose of transferring key technologies of the 0.18㎛ design-rule 256Mb SDRAM device to the plant for mass production. Achieved overall yield 60% in the mass production line.

Jan/94 ~ May/97 Rinnai Korea Cooperation ***Engineer – Electronic Ceramics Team, R&D Division***

- Developed SAW filter devices for communication and high-k materials such as PTC, NTC and PZT for semiconductor sensors.
- Designed, created and installed the new sorting machine in production line, resulting in 10% cost savings.

核心技术

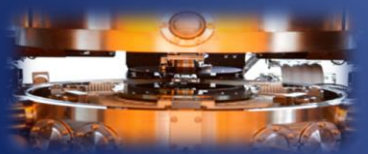


差动技术比较

技术	加热 (Heating)	调整 (Alignment)	表面处理 (Surface Treatment)
LTRIN	RF Heating (Max. ~550℃)	Align and Bonding simultaneously in the Chamber (Without Chuck)	Cleanable Plasma (1 step process)
竞争公司	Resistance Heating (Max. < 400℃)	Align + Bonding Module (AP only)	Vacuum Plasma (2 step process)

与其他竞争公司相比拥有能提供优质生产效率标新立异的技术。

制品：Permanent Bonder Ⅰ



Heating

Type：RF Induction

Performance：Range < 500℃ (Max. 550℃)

Heating Rate > 200℃/min (Controllable)

Uniformity ± 1%

Pressing

Type：Servo Press

Performance：Max. 60KN

Uniformity < 2%

Alignment

Type：In-situ alignment and bonding

Performance：Align Accuracy < ± 1.0um

性能

Item		Performance		Remark
		Competitor	Morian200RA	
General	Wafer Size	4~12”	4~12”	-
	Number of Chamber	Max. 4	Max. 4	-
	RGA port	NO	YES	-
	Number of Gas port	-	4 Port	N2, He, Ar, Forming Gas, etc.
Align	Type	Alignment + Bonding	In-situ Align and Bonding	-
	Align Accuracy	≤ ±1.0㎛	≤ ±1.0㎛	-
Heater Module	Max. Temperature	550 ℃	550 ℃	-
	Max. Heating Rate	< 35 ℃/min	> 200 ℃/min	Controllable
	Temperature Uniformity	5 ~ 10 ℃	< ±1%	-
	Control of cooling rate	NO	YES	-
Pressing	Max. Pressure	50KN	60KN	Option : 100KN Available
	Pressure Uniformity	< 2%	< 2%	-
Vacuum Chamber	Vacuum Capability	≤ 1 x e-5 mbar (7 x e-6 torr)	≤ 1 x e-5 mbar (7.5 x e-6 torr)	-
	Pressurized Capability	No	YES	< 2,000 torr (2.3 ATM)

制品 ：Permanent Bonder Ⅱ

Wafer Direct Bonding System

LTRIN

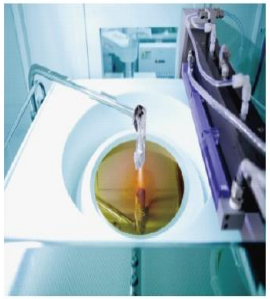
Model : LTRIN3000

▶Cleanable Plasma & Cleaning Hybrid Module

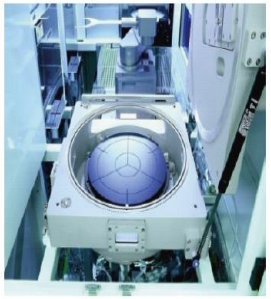
- Particles removal by nano-spray
- Cleanable A.P plasma for surface treatment (orgaric particle removal)
- Substrate modification from hydrophobic to hydrophilic surface

▶Wafer Bonding Module

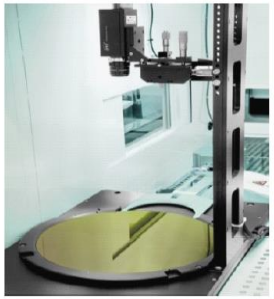
- Auto mechanical alignment in the chamber
- Room temperature process
- Low vacuum pressure
- 8" ~ 12" wafer compatible



Cleanable Plasma & Cleaning Hybrid Module



Wafer Bonding Module



IR Inspection Module

▶Specification

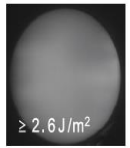
✓Void-free bonding

✓Grinding / CMP acceptable high bonding strength (≥2.3 J/㎡)

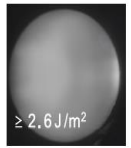
✓Throughput : ≥ 20wph

✓Auto defect-inspection System

▶Defect-free & High Bonding Strength

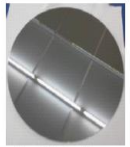


Ox/Ox Bonding



Ox/Si Bonding

SOI Wafer



After Thinning Process

- Remain Silicon : 60㎛
- No Defect after Thinning
- High Bonding Strength

制品 ：Temporary Bonder

Model : LTRIN2000A

▶Wafer Level Package Bonding System

- Auto mechanical align in the chamber
- High thermal process (≤400℃)
- High vacuum (ATM~10^{-6} torr) process
- Anti-contamination system against out-gassing
- Auto pressure optimization system

Wafer Bonding Module

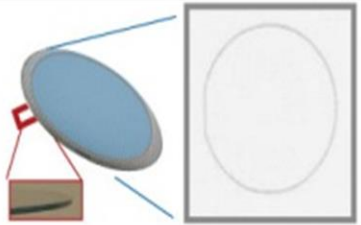
Auto EFEM Module

High Transfer Robot

▶Specification

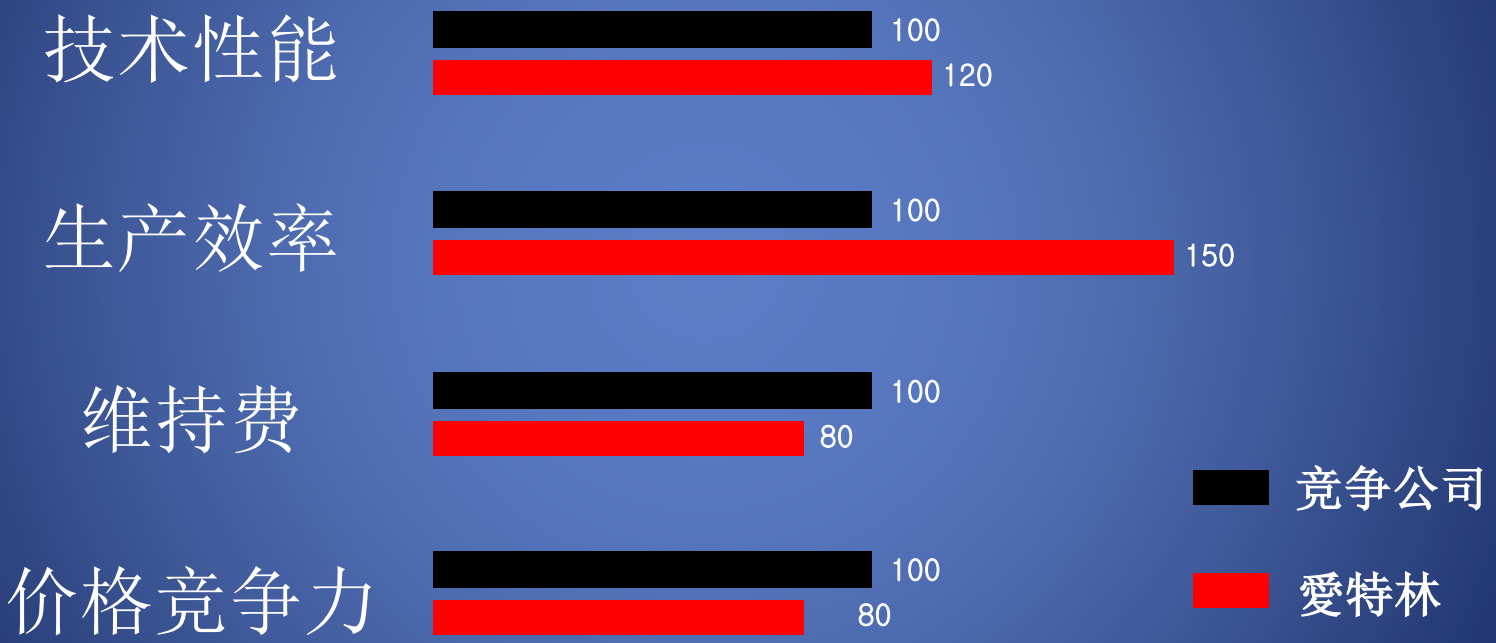
- ✓Void-free / Anti-scratch bonding
- ✓Grinding / CMP acceptable high bonding strength
- ✓Max. process temp : ~400℃
- ✓Max. process force : 100KN
- ✓Temp. uniformity : ≤ ±1%
- ✓Pressure uniformity : < ± 5%
- ✓Easy maintenance by simple cluster type system

▶Defect-free Image



- ·No void / No pattern collapse
- ·Glass / Patterned wafer bonding with the adhesive film

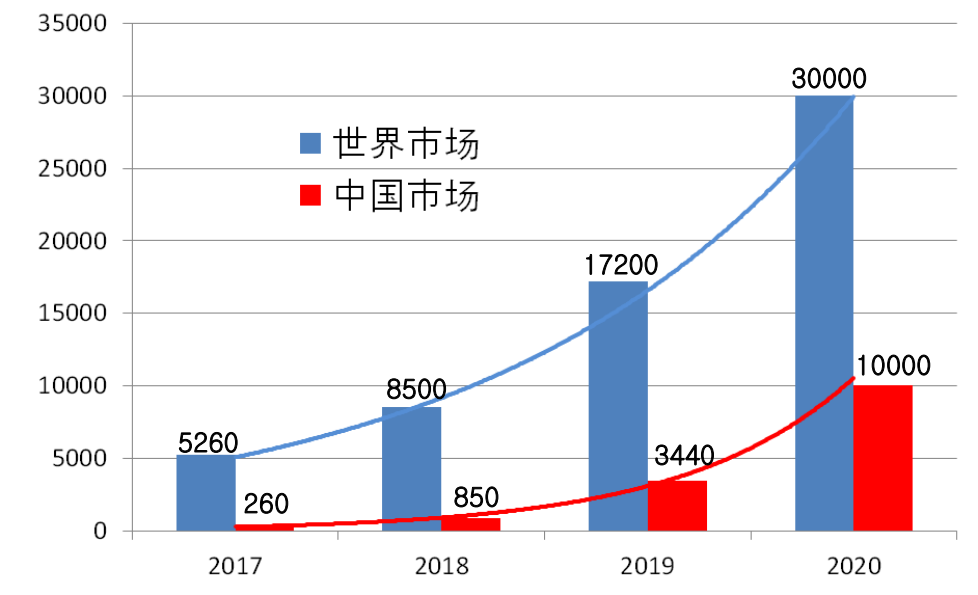
产品竞争力



在中国业务战略

Wafer Bonder 中国市场展望

(M RMB)



世界市场（中国以外）

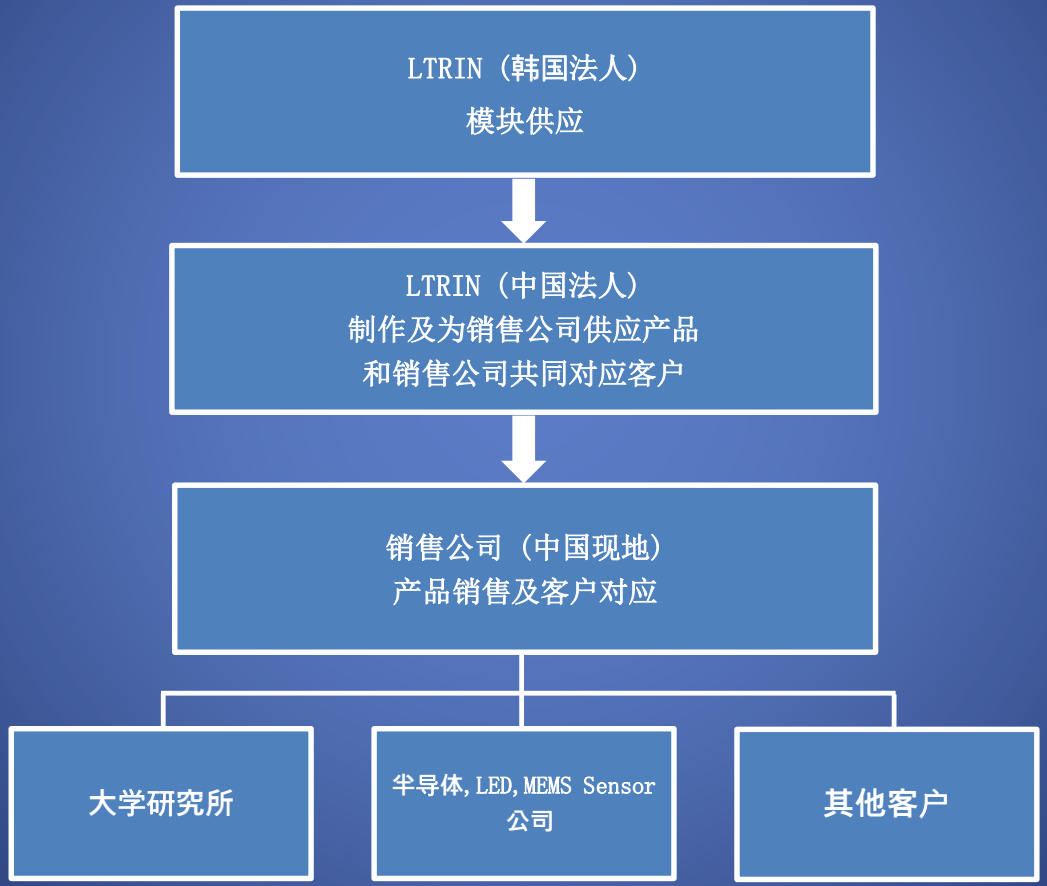
来源：*Yole Development*

中国市场（预计）

(M RMB)

区分		2017	2018	2019	2020	Remark
世界市场	*中国以外*	5260	8500	17200	30000	来源：Yole
中国市场	*中国/世界*	5%	10%	20%	30%	预计
	预计	260	850	3440	10000	

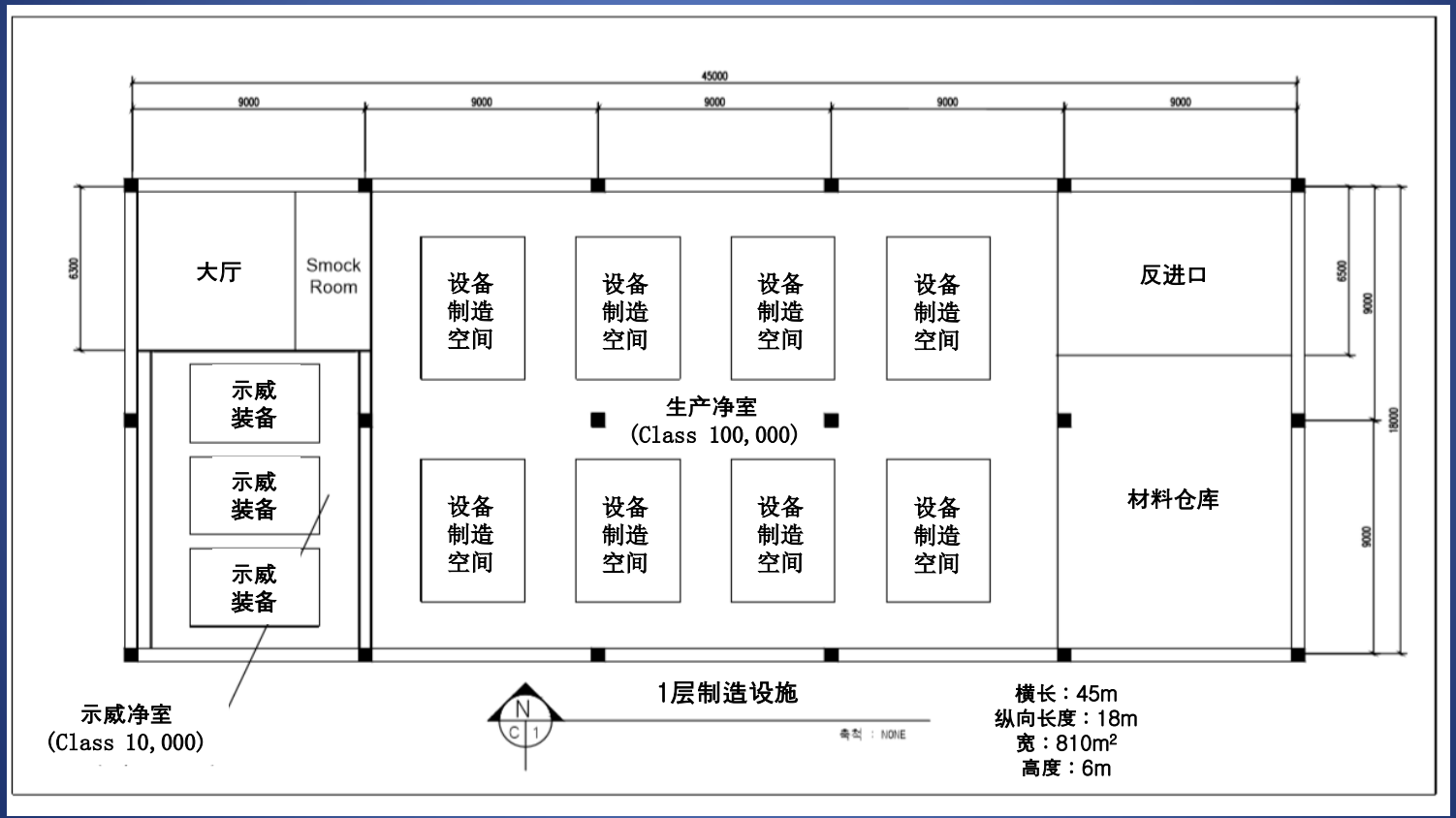
事业推进战略


LTRIN（韩国法人）
模块供应
LTRIN（中国法人）
制作及为销售公司供应产品
和销售公司共同对应客户
销售公司（中国现地）
产品销售及客户对应
大学研究所
半导体,LED,MEMS Sensor
公司
其他客户

人员保障战略

业务领域	所需经验	人员（名）			
		设立初期	Phase I (2020年)	Phase II (2021年)	Total
代表理事	专业经营人	1	-	-	1
技术责任人	半导体/MEMS工序技术&机械设计	1	1	-	2
技术营销	半导体/MEMS工序技术&精密机械制作	1	2	5	8
技术工程师	半导体/MEMS工序技术	2	5	7	14
设计工程师	2D/3D CAD设计，理解真空原理	2	5	8	15
电气工程师	电路设计及电气工学	1	3	5	9
(S/W工程师)	Multi Tasking & C++, PLC 控制	1	3	5	9
装配技术员	精密机械装配，运作技术	4	6	8	18
职员	税务，会计，总务	1	1	2	4
合计		14	26	40	80

制造设施


45000
9000
9000
9000
9000
9000
6300
大厅
Smock Room
设备制造空间
设备制造空间
设备制造空间
设备制造空间
反进口
6500
9000
18000
9000
示威装备
示威装备
示威装备
生产净室
(Class 100,000)
设备制造空间
设备制造空间
设备制造空间
设备制造空间
材料仓库
示威净室
(Class 10,000)
N
C 1
1层制造设施
축척 : NONE
横长：45m
纵向长度：18m
宽：810m²
高度：6m

谢谢

www.ltrin.co.kr